

FIG. 1

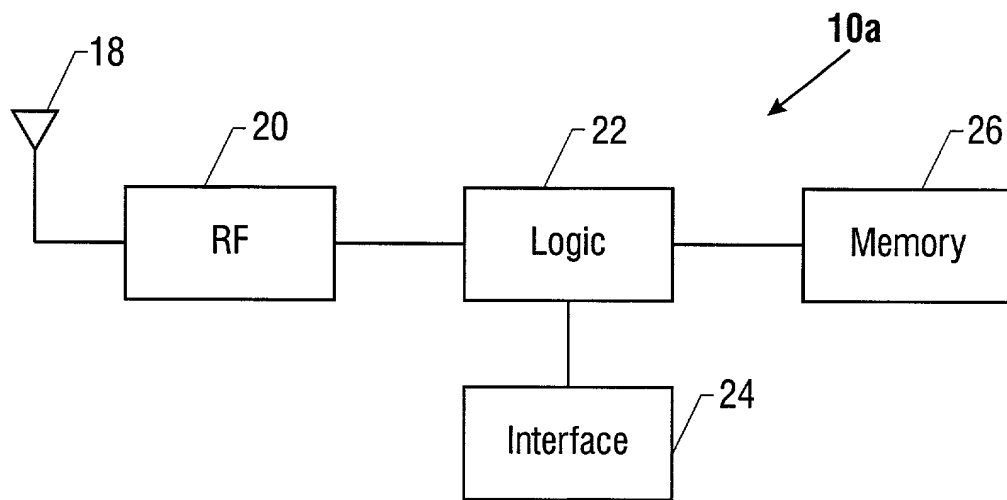


FIG. 2

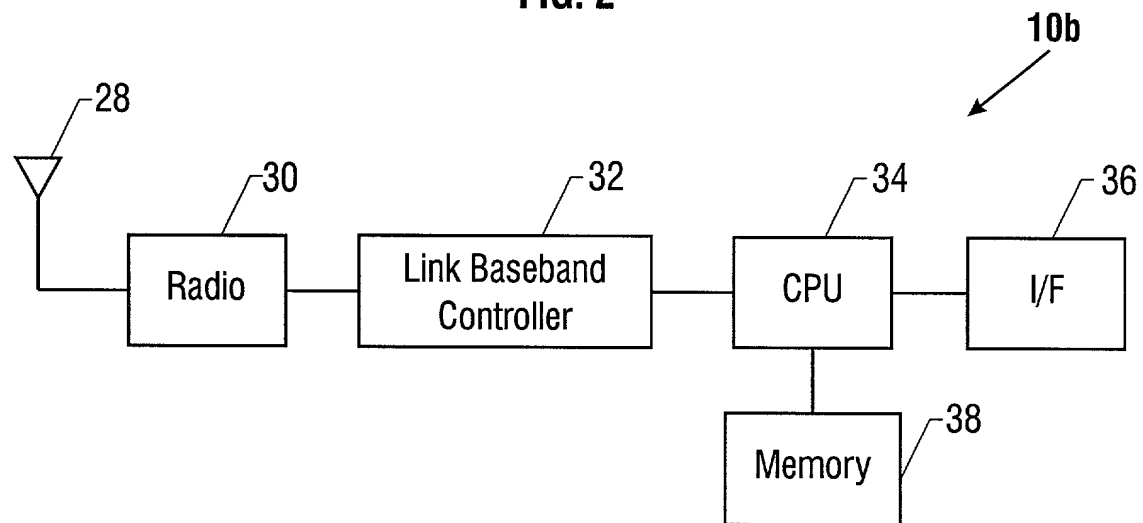


FIG. 3

FIG. 4 is a cross-sectional view of a semiconductor device in accordance with the present invention.

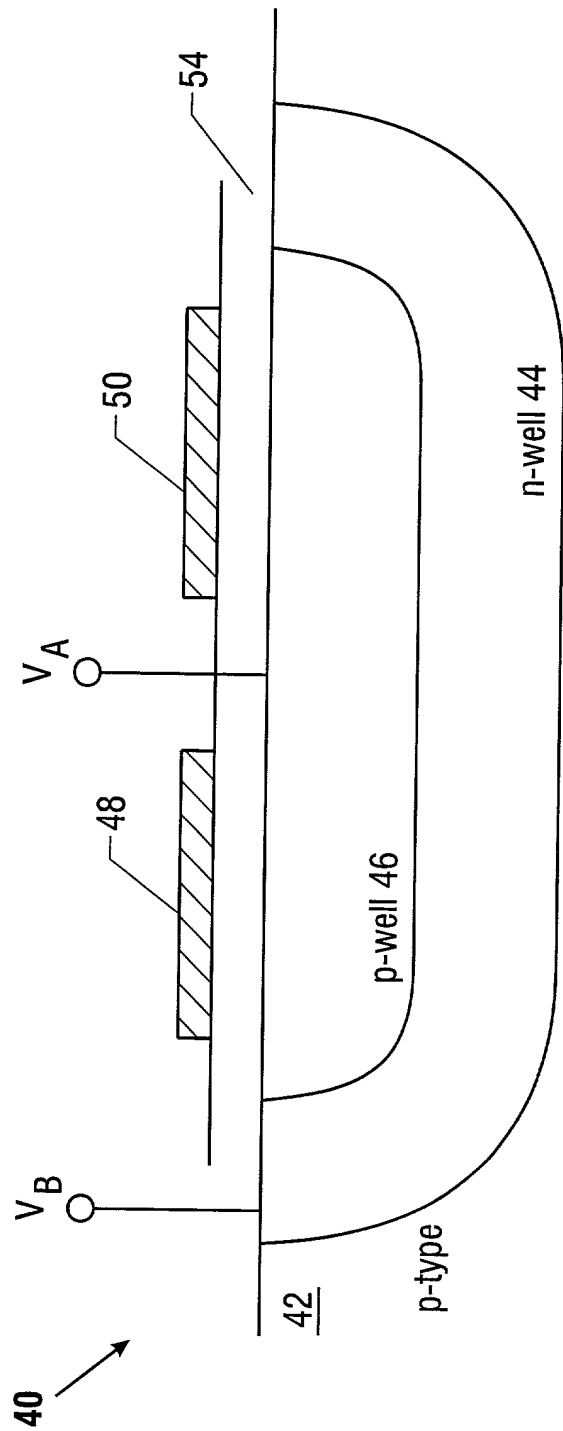


FIG. 4

FIG. 5

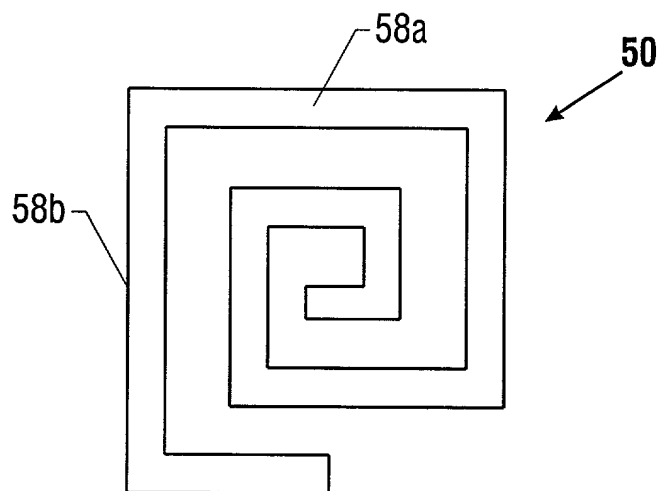


FIG. 6

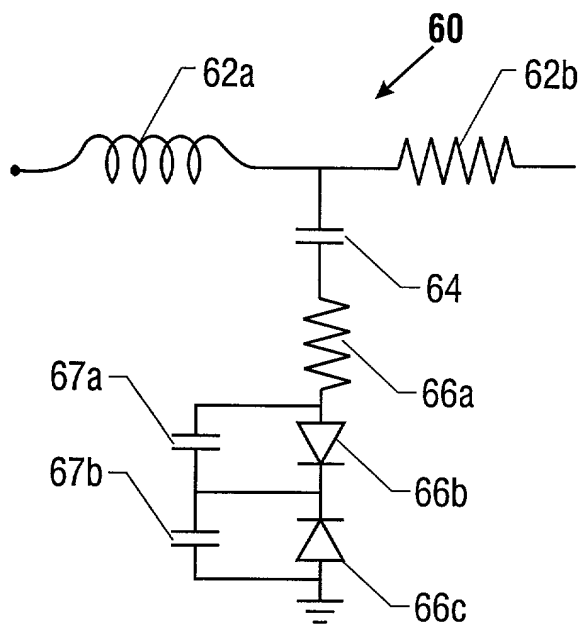
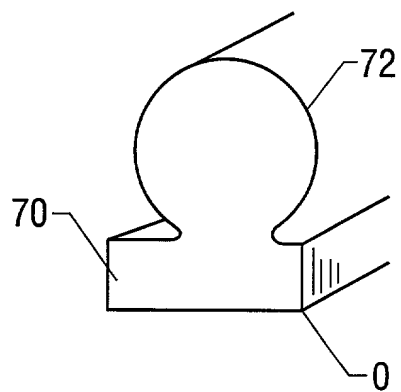


FIG. 7



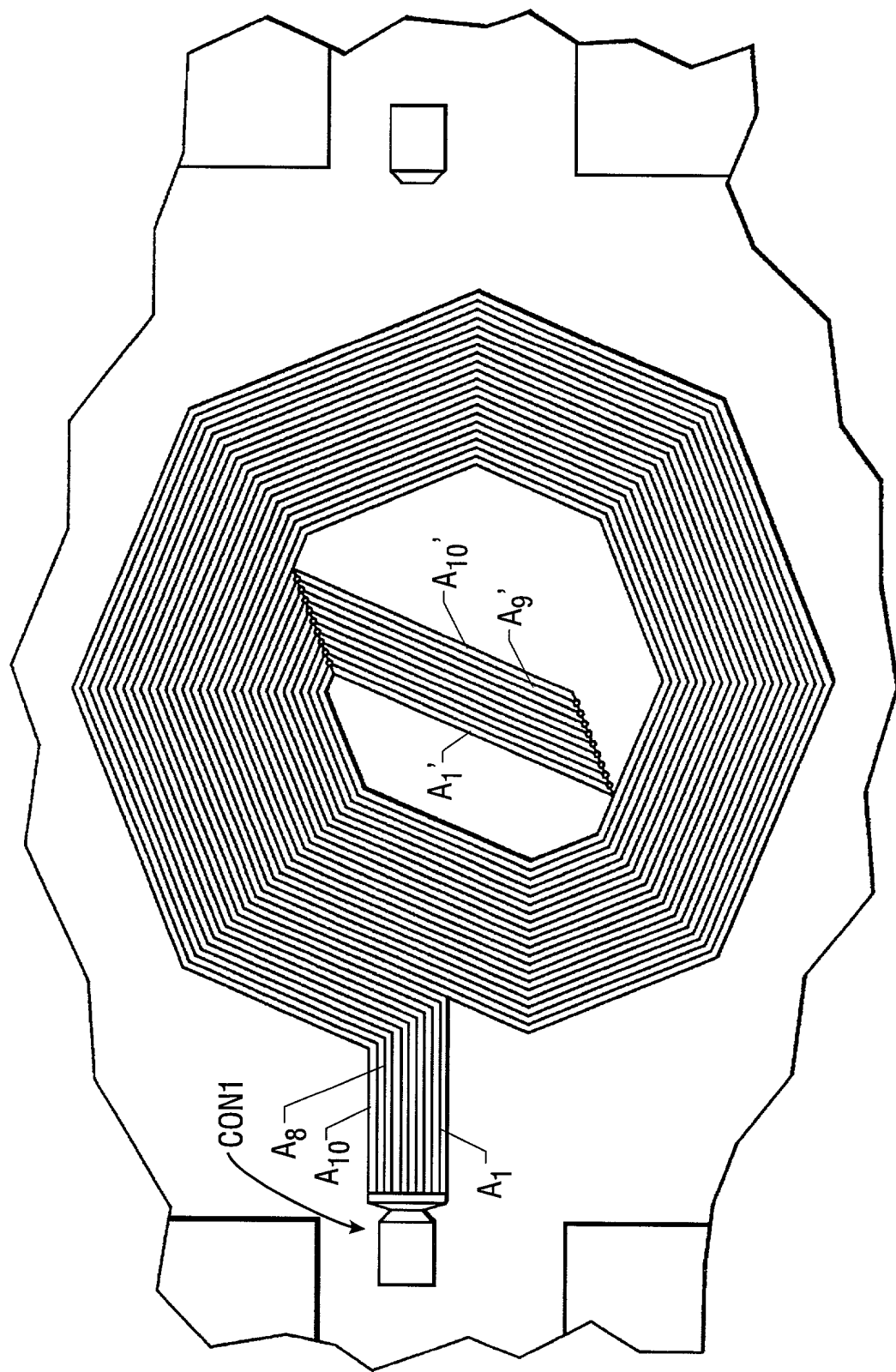


FIG. 8A

FIG. 8B

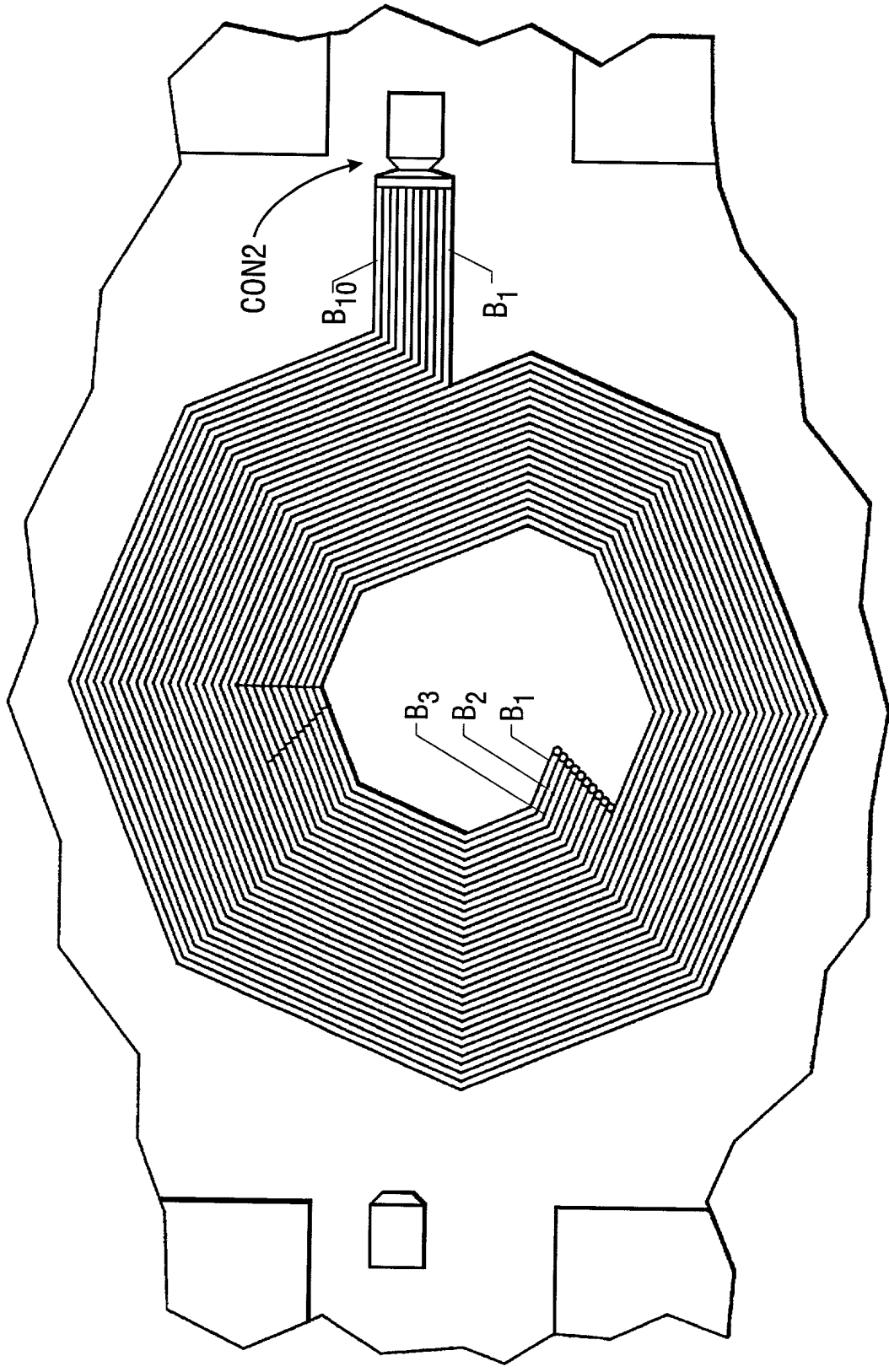


FIG. 8B

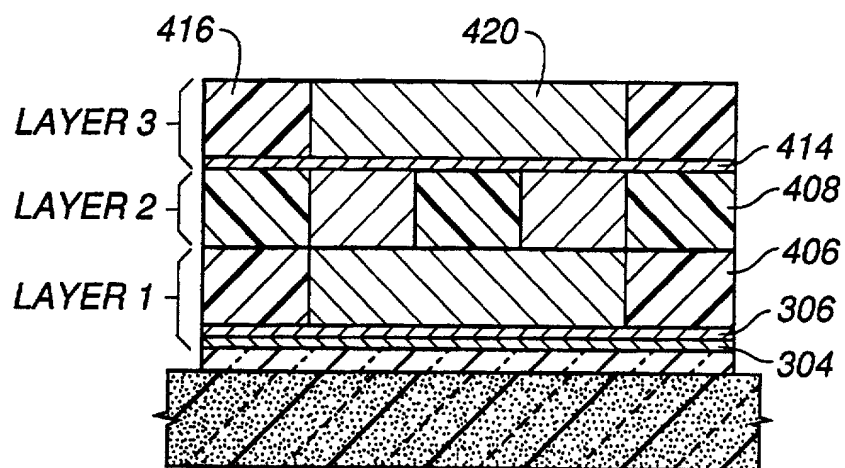


FIG. 9

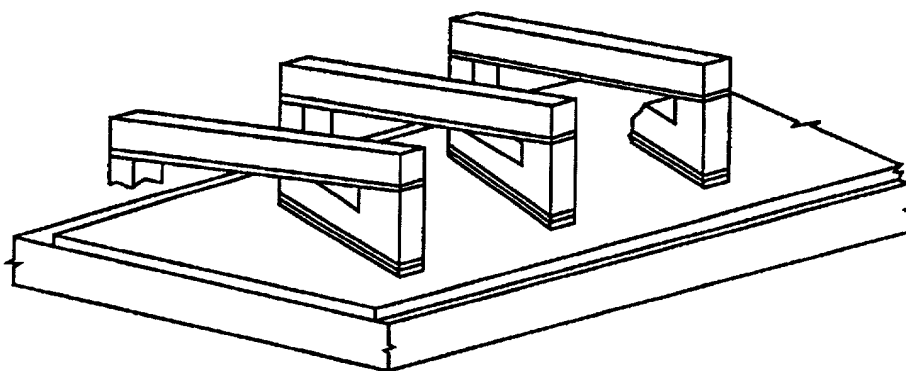


FIG. 10

450

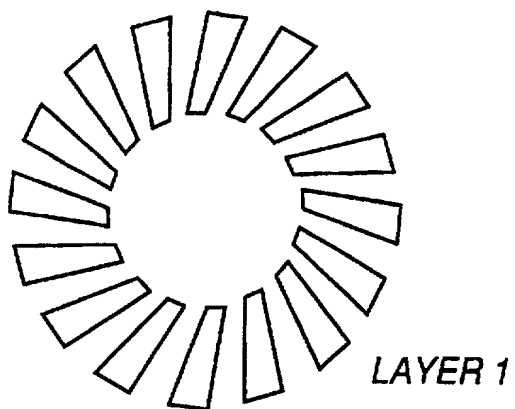


FIG. 11

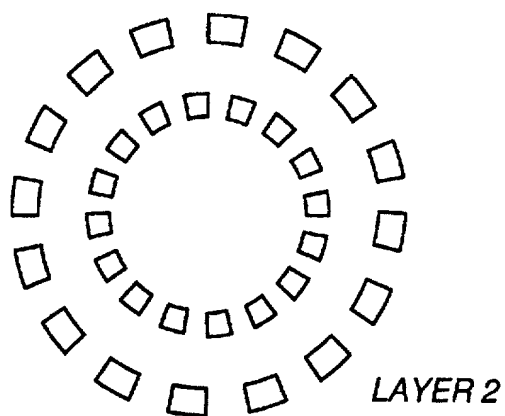


FIG. 12

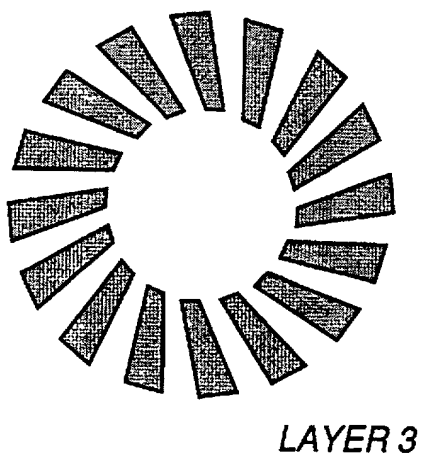


FIG. 13

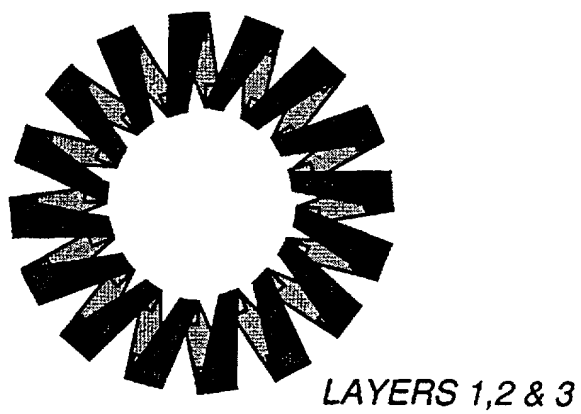


FIG. 14

FIG. 15 is a schematic diagram of a device 100, including a first antenna 50a, a second antenna 50b, a third antenna 50c, a fourth antenna 50d, a fifth antenna 50e, a first antenna array 80, a second antenna array 82, a first antenna array 86, and a second antenna array 88.

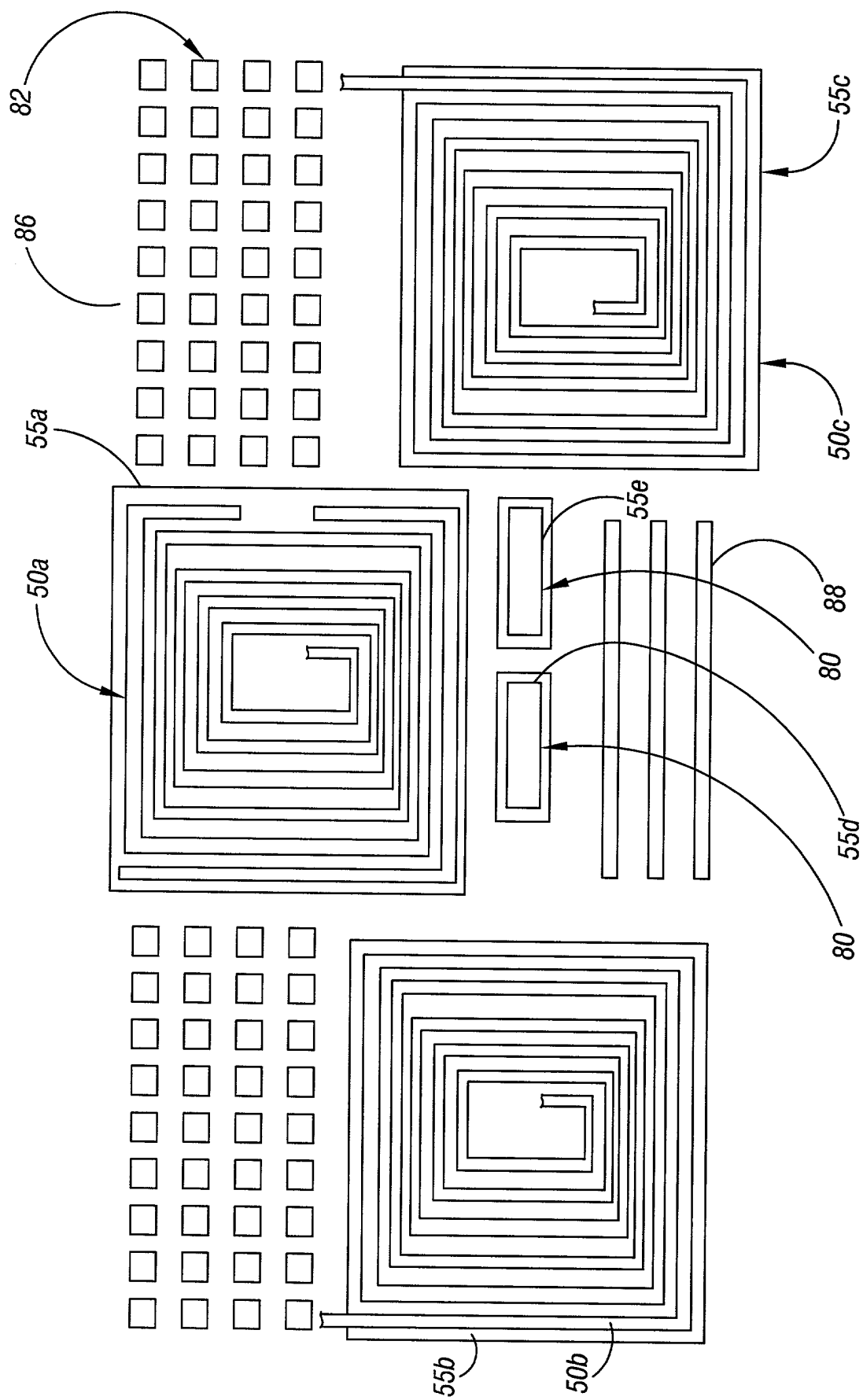


FIG. 15

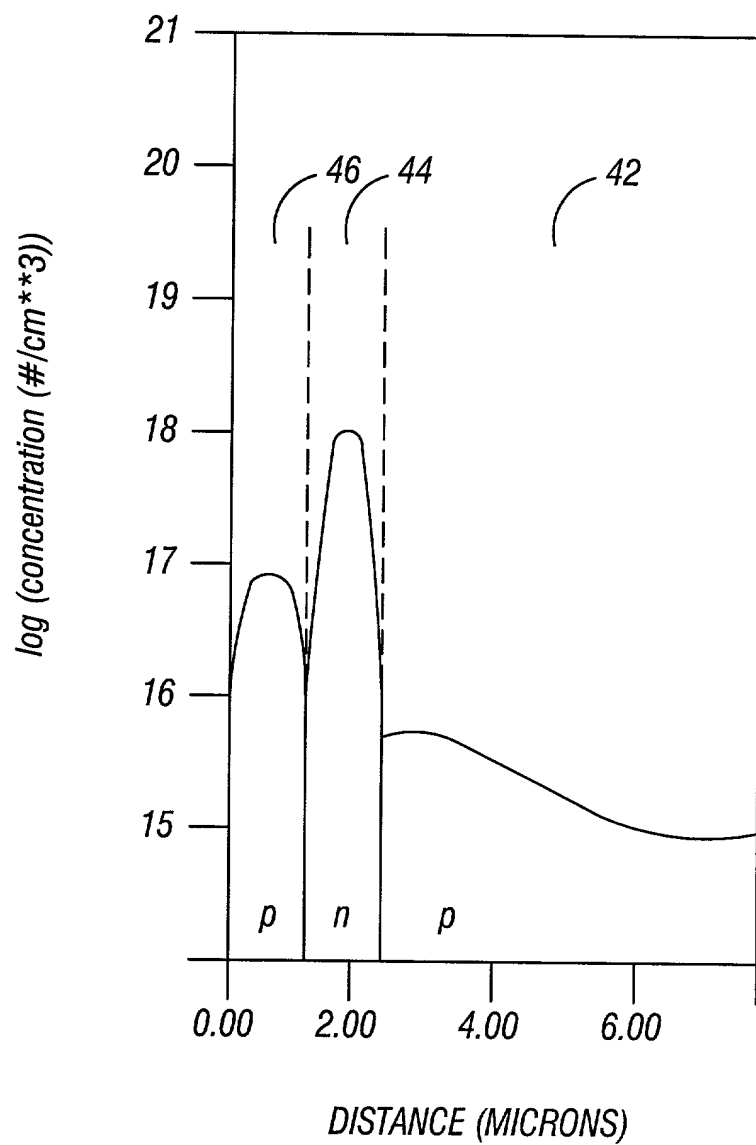


FIG. 16

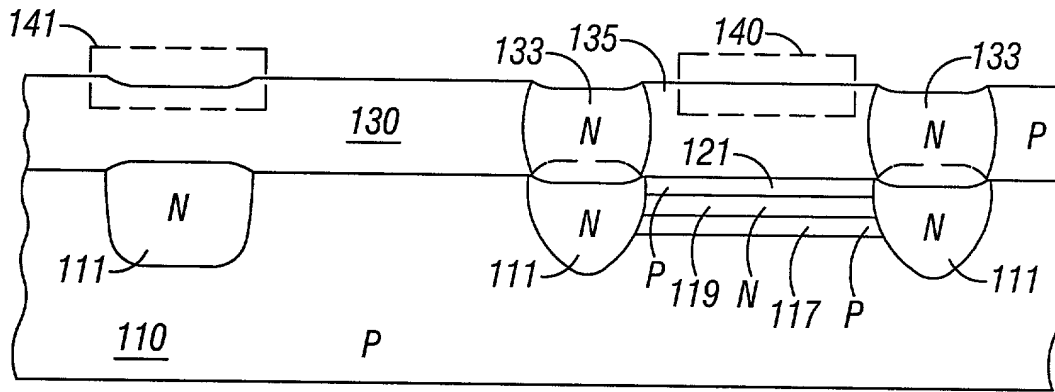


FIG. 17 (PRIOR ART)

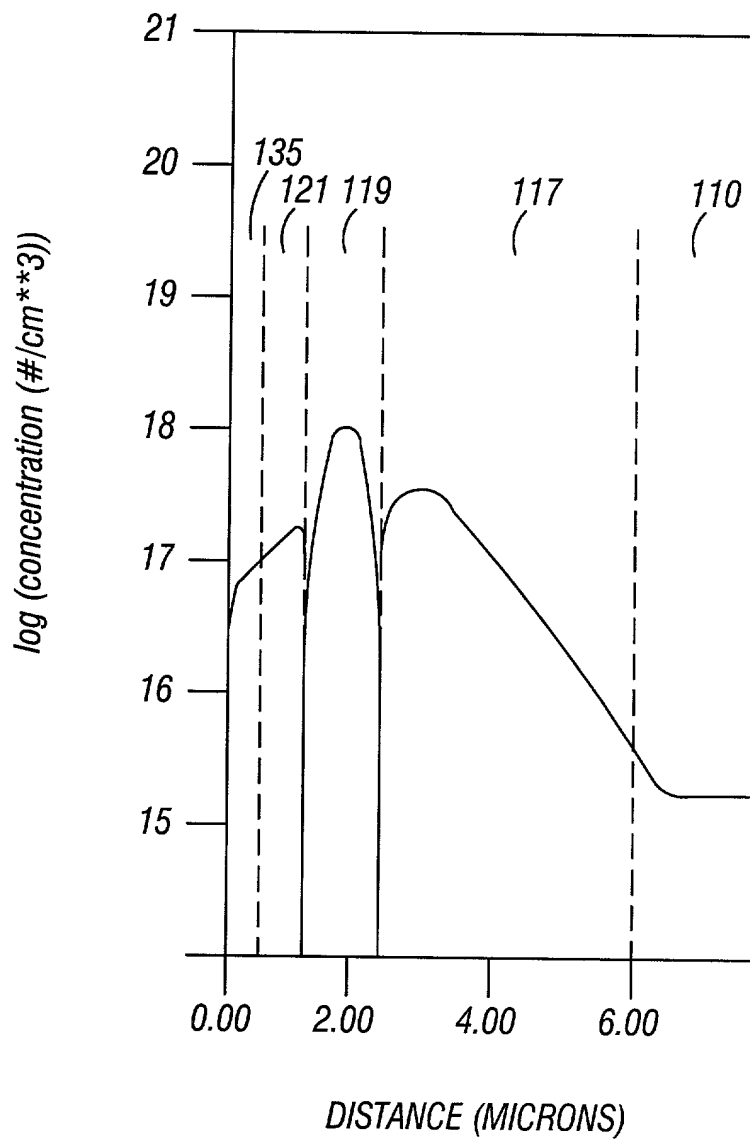


FIG. 18 (PRIOR ART)

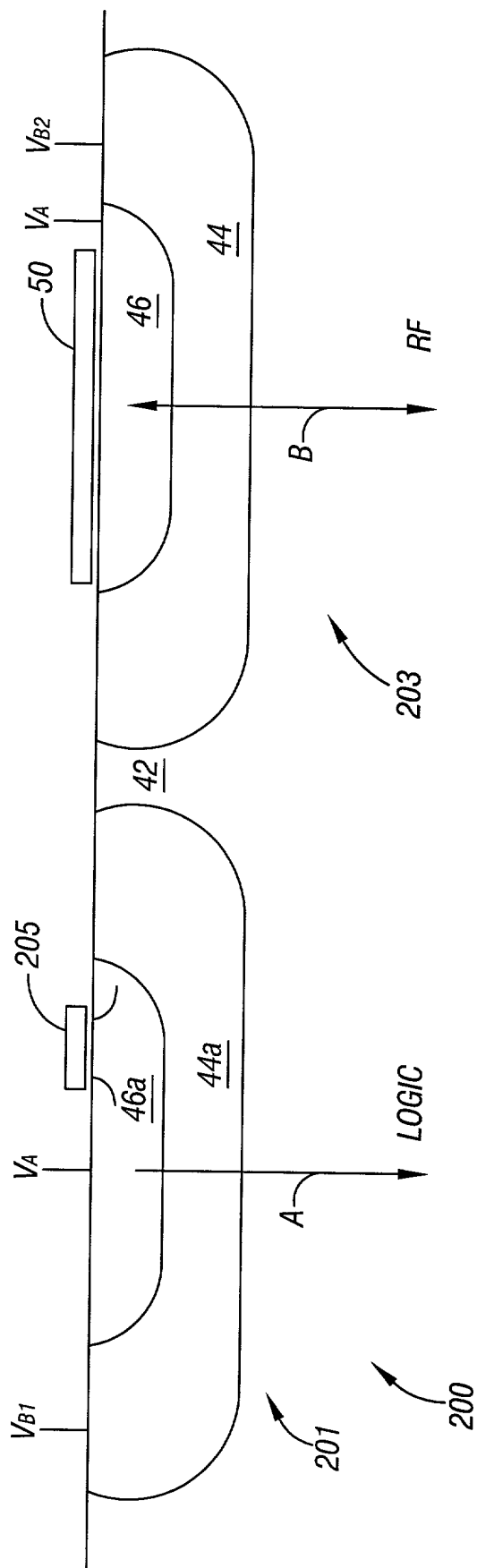
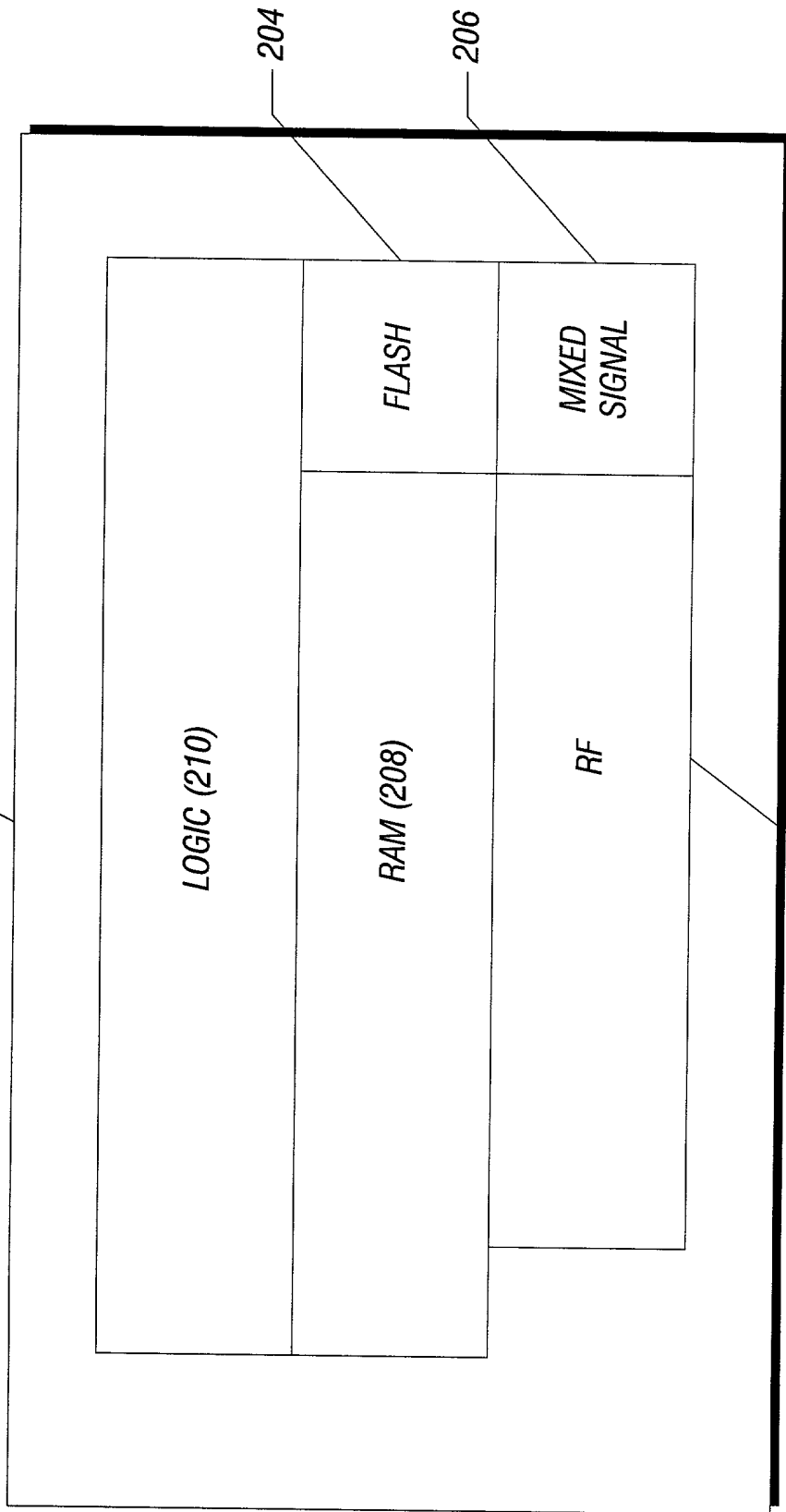


FIG. 19

200



203

FIG. 20

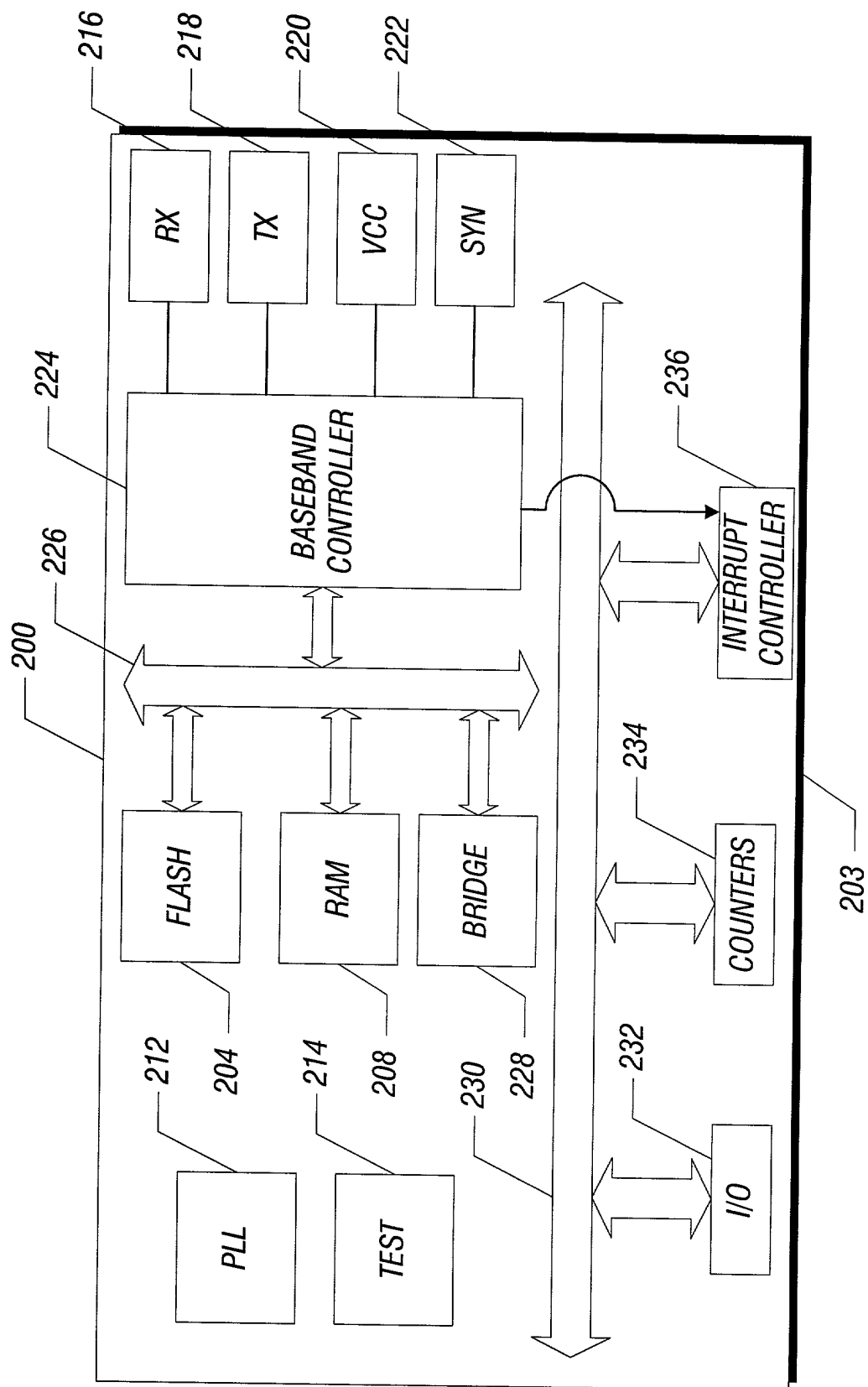


FIG. 21

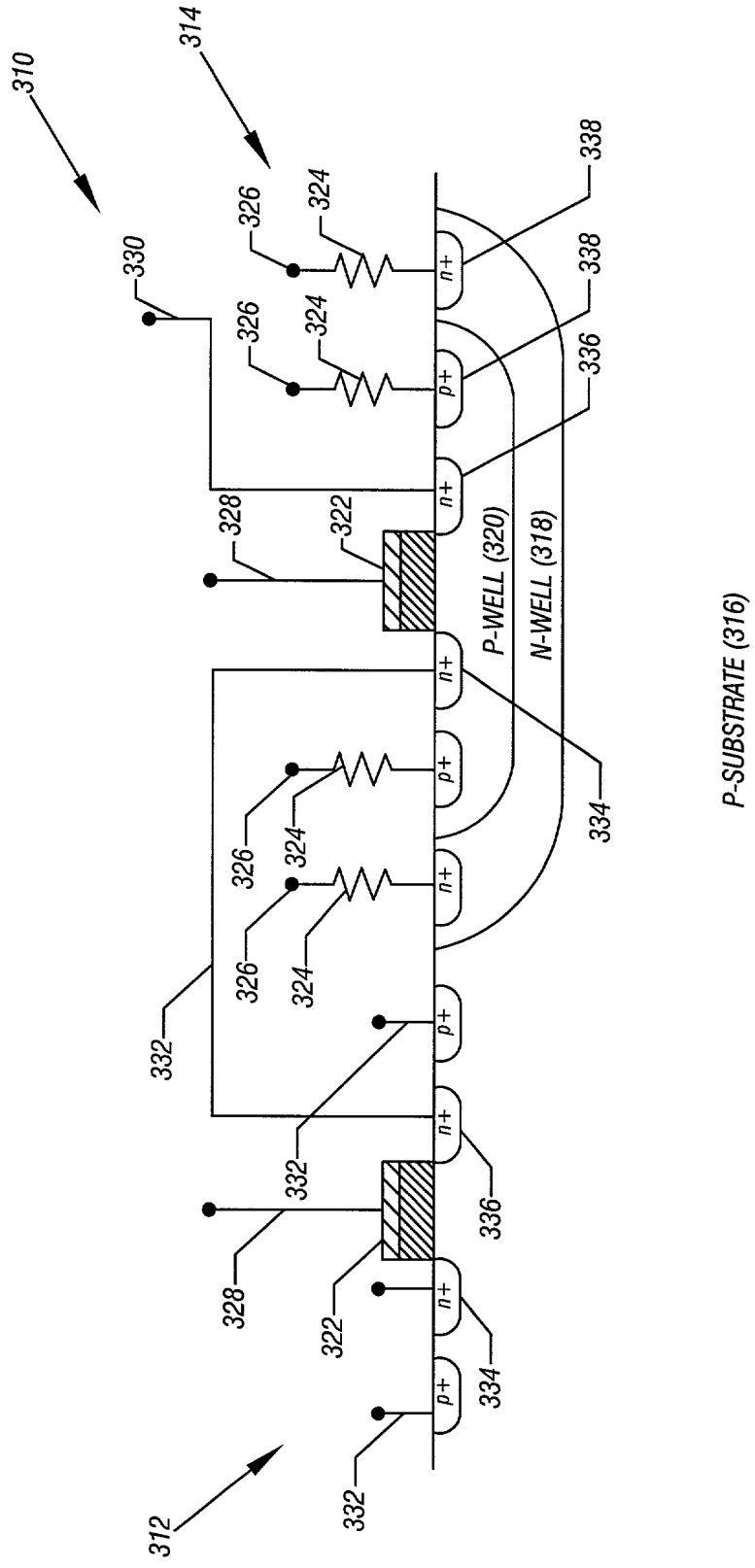


FIG. 22

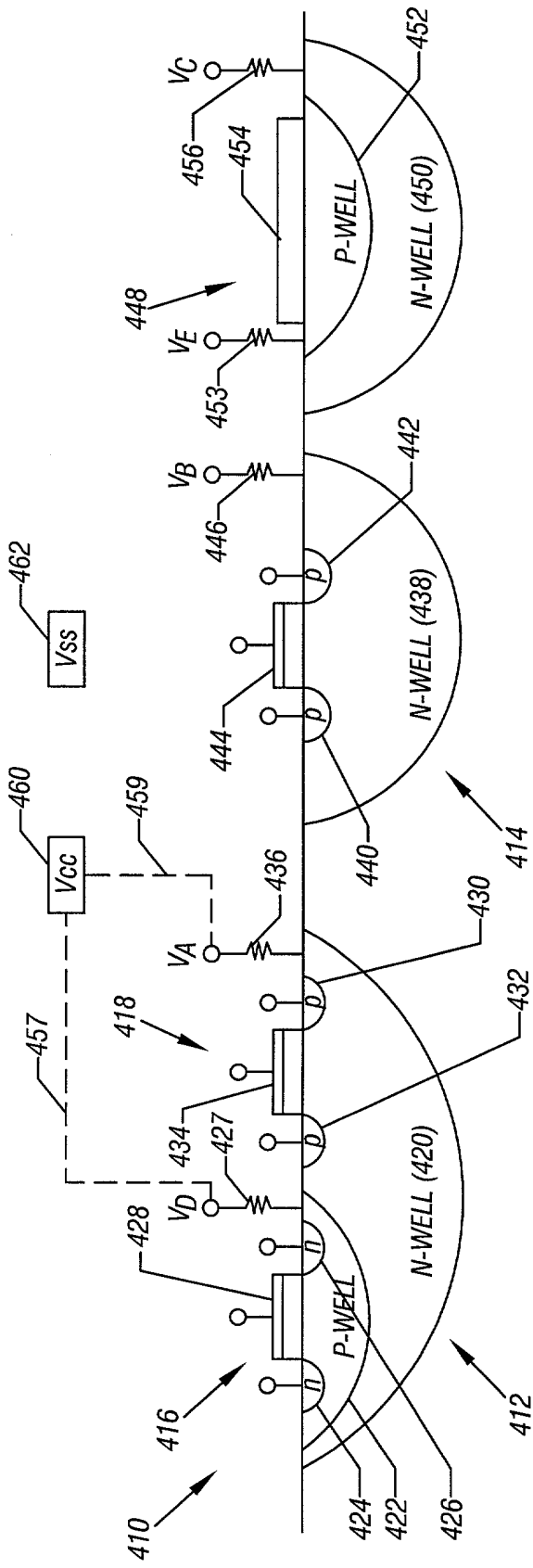


FIG. 23

P-SUBSTATE (448)